IN THE UNITED STATES DISTRICT COURT
MIDDLE DISTRICT FOR TENNESSEE

TIMOTHY ALLEN ATCHISON	)
	)
Plaintiff,	)
	)
v.	)
	)
	)
HUBBELL INDUSTRIAL CONTROLS, INC.	)
	)
Defendants.	)

ATCHISON COMP. EX.1

PATENT DOCUMENTS

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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
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Title of Invention

Multipurpose Automatically Compensating High Power Switching Transistor Transient Protector

Application Information

APPLICATION TYPE	Utility - Provisional Application under 35 USC 111(b)	PATENT #	-
CONFIRMATION #	9408	FILED BY	Timothy Atchison
PATENT CENTER #	63687671	FILING DATE	-
CUSTOMER #	-	FIRST NAMED INVENTOR	Timothy Atchison
CORRESPONDENCE ADDRESS	Timothy Atchison 353 Sunset Island Trail Gallatin, TN37066	AUTHORIZED BY	-

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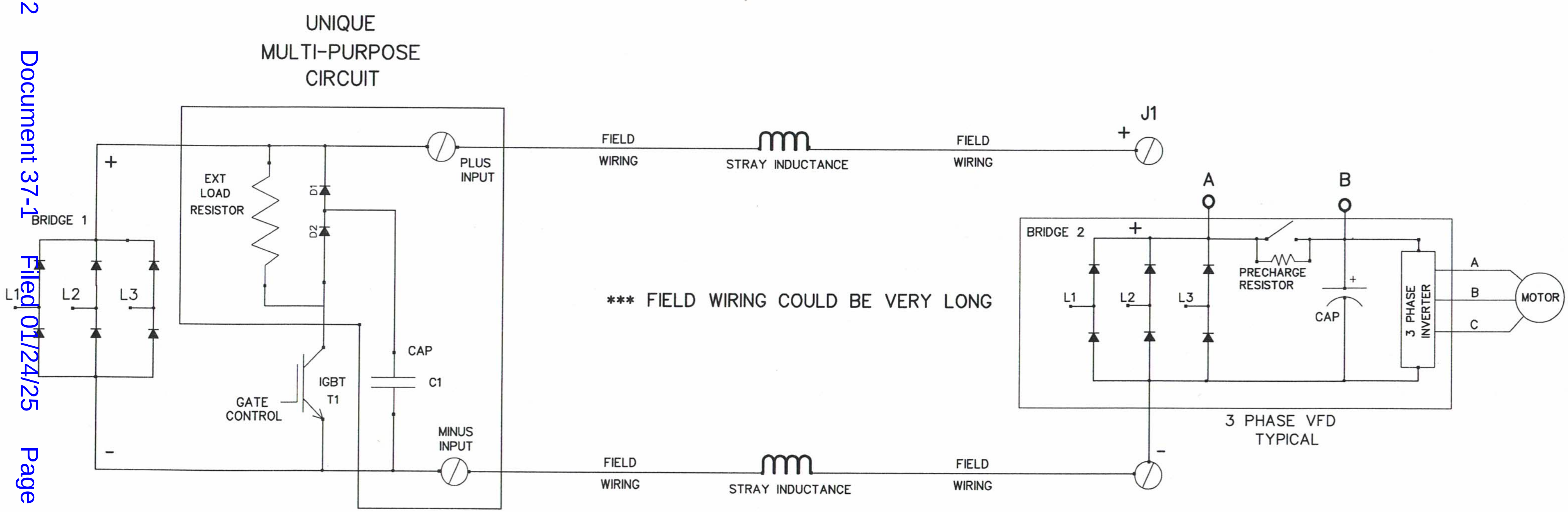
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Multipurpose "Automatically Compensating" High Power Switching Transistor Transient Protector

Preface: In order to be as "power efficient" as possible, *every* "switching" transistor *must* switch current flow from "off to on" and "on to off" in the absolute least amount of time possible. This is especially true in the case of the very high current and high-power transistors. The transistor workhorse in the world of today is the "IGBT transistor". It is optimized for high-speed switching of high power. However, turning on high levels of current flow fast (as you must to be efficient), then interrupting this current flow "fast" (as you must) can easily create destructive very high voltage spikes (transients), which left unaddressed can easily exceed transistor voltage ratings, leading to device failure and likely **very loud** *high energy destructive explosion*. Thus, every transistor switching circuit must employ some means of mitigating these destructive switching transients.

In the accompanying drawing, you will see *a Very Unique Circuit* that I conceived that addresses this particular problem/requirement, *but also has **other** very important and useful functions and benefits.* This Unique Circuit is suited for and beneficial in a variety of Power Electronic control circuits, with many complex power topographies/distributions, even within a given application, such as Heater Control, AC Motor Control, DC Motor Control, to name a few.

As an example, in the drawing, to gain understanding, the Unique Circuit is employed within a Dynamic Brake Unit (DBU) for use in AC motor drive systems to assist in motor stopping or periodic overhauling motor loads (regenerative).

For Reference: A DBU comprises a switching shunt voltage regulator, used in the presence of regenerated energy (emitted from an operated motor) under conditions that cause it to create vs consume power, the motor being controlled by (typically) a 3 phase AC Variable Frequency Drive (VFD). Regulating, the DBU switches an energy absorbing resistor on and off at a rate and duty cycle (to precisely convert to heat) the precise amount of power emitted from the motor. In our drawing, during regeneration, all AC Line Bridge Rectifiers are off (not conducting).

In ideal power circuit designs such as employed in the traditional VFD Motor Controller (with embedded inverter section), very low capacitive impedance and very low inductive impedance surrounds the motor switching transistors which automatically and inherently minimizes switching transients. However, there are many applications and variations thereof, wherein this cannot be the case.

For comprehensive and illustrative purpose, let us consider the typical VFD motor controller shown in the drawing, with respective power circuitry. Using careful and strategic designing, it is not difficult to locate the Inverter Section transistors physically (thus electrically) close to the capacitance bank (typically pretty high value), which is mandatorily present to filter the output of the AC/DC rectifier section **(Bridge 2)**. Any other capacitance (if needed at all) would be minor. Simply because the main capacitors must be present, enables them to serve a dual role. Of specific importance, make note especially of the **mandatory** pre-charging circuitry (post rectifier contactor or relay and dedicated specific purpose charging resistor) that **must** exist to get the bulk capacitor banks charged from zero volts up to 850 Vdc (in 3 phase 600 VAC mains systems) upon applied power.

Main: As stated, there are **many switching** transistor module applications and circuitries that *cannot* make use of such main capacitor banks that otherwise exist, and to implement/include such within the module would add **significant cost, weight, size and circuit complexity**, which all represent competitive **disadvantages.** In such power (and high power) applications, it simply boils down to the fact that these modules *cannot be* (<u>or there is strong preference for them not to be</u>) physically located near the main pre-existing system capacitance banks…. *yet still need transient protection, still need capacitance, and still need a means of charging such capacitance.* **As but one** example is in the drawing shown. *To address such needs, whilst greatly conserving the critical competitive factors (listed above)* I conceived **this very unique and specialized** circuit which provides **self-compensating, dampened** transient protection plus much more ***all while utilizing only a few components!***

*I am aware of switching power module applications being sold in the world today, that may need to be located quite some distance from the main system DC Bus (and thus capacitor banks) that **mandatorily** require the purchase of an "ADD ON MODULE" to provide compensational/protectional needs. *If this is not done, failure of transistor is likely and normal operation cannot be relied upon.* ***"This approach" requires extra back panel space, significant cost adder, and one more item within which failures can occur, making the overall MTBF picture worse!***

Features/Benefits/Advantages of the Conceived Circuit

- Reduced system cost
- No mandatory "add on" modules to purchase to achieve safe, normal operation of external controller (DBU in this case) *which may only be recognized as needed after a first costly failure.*

- Reduced system circuitry complexity: no monitoring circuitry of capacitor **C1** (to be charged up at power up) nor shunting contactor necessary, *nor even a resistor to charge C1.*
- No mechanical device associated risks: (contactor or relay) which has finite switching life cycle, that could fail (stuck/welded shut or stuck open contacts, or corresponding coil to burn out). If contacts were to weld/stick shut, the next power up sequence would likely blow system fuses, or breakers, and components housed in the VFD (or DBU) (in this example).
- *In dual role manner*, automatically makes use of system energy absorber resistor (or heater controller element or other power consuming load) to provide capacitor necessary/required pre-charging function at power up, whilst also including *same resistor* on a cycle by cycle switching basis (T1) to provide damping function in turn on/turn off switching transient mitigation.
- Eliminates need for additional/other smaller resistor (albeit still sizable/normally needed) to help in turn on/off damping of switching transients generated on cycle-by-cycle pulse train basis (resistive component alleviates ringing)
- **Very Importantly,** automatically allows and provides inherent ability of power module (DBU in this case) to be located a long distance away from main/bulk system capacitance (VFD), whilst maintaining transient mitigation.
- **Automatically** compensates for the inherent inductive impedance (during power up) in the AC line side (**Variant 2** below in this example) which could be simply the feed transformer impedance and or line reactors (for improved power factor purposes) into the 6 pulse 3 phase bridge rectifier **(Bridge 1)**.
- **Very uniquely and automatically** compensates in the transient mitigation function (in the switching mode turn on/off operation **(T1)** on a pulse-by-pulse basis) for the inherent inductance (stray inductance accompanying any wire, **proportionately higher the longer the wire**) in the DC link in this figure, between the VFD DC Bus and the power module under discussion, *as well as all inductance in the R load and wiring.*
- **Because of certain aspects of its unique functionality,** C1 can be much smaller in terms of its microfarad value (than would otherwise be needed), which saves (DBU) module cost, module chassis size/space, backplate space.

IMPORTANT NOTE: In the VFD motor controller figure, the rectifier Bridge 2 output **(point A)** may be *the only point of access* to the outside world for the DC +, rather than

point B. In this case, any externally connected DBU will experience a DC voltage step function at power up; potentially and likely damaging to a standard configuration DBU (capacitance connected directly across +/- input) and/or VFD (Bridge 2 or blowing of AC fuses/breakers feeding Bridge 2) vs. the gradual exponential RC ramp up in voltage found at point B. The ramp up nature of this node voltage will not harm typical power module, AC line fuses, or rectifier diodes.

System Variations: Sticking with the VFD example, there can be multiple configurations/variations that exist where the Unique Circuit I conceived exhibits its functional benefits. Let us first examine to understand the automatic precharging benefit (*amidst these variations*), which will prevent and avoid failures.

Variation 1: In the first variation, **Bridge 1** would be absent. There would be only (1) VFD. There is no way to know for sure if the VFD has **point A (+)** (there are good reasons to bring out **point A**) brought out to connect to **(J1)** rather than **point B**. *Or both points could be brought out for customer connection.* Point **B** would be the preferred point to bring out for a traditionally wired/standardly available externally connected DBU which relies on the (its) applied DC voltage ramping up slowly, so as to ramp up its own internal capacitors slowly. Note: *It is common for a conventional DBU to have local capacitance for transient mitigation wired directly across its DC plus/minus (like the VFD once the charging contactor closes).*

- It should be clear that if point B is connected to a DBU of this type (via J1), that at power up, there would be no problem. The DBU capacitors just ramp up at the same rate as the VFD capacitors.
- However, if point A is connected to the DBU when power is applied, *<u>there will be a big problem</u>* trying to charge the DBU capacitance instantaneously to full voltage output of Bridge 2 without any charging resistor whatsoever!! Remember, capacitors initially appear as short circuits and must be charged through a current limiting resistor! *Short circuit currents will flow in this mode of power up, that could damage Bridge 2, blow its line fuses or breakers, or damage the DBU!*
- Not to mention, charging through the inductive source impedance (feed transformer windings, DC wire length inductance etc.) would charge the conventional DBU capacitors to up to **twice** the (no load) peak output voltage of Bridge 2 due to LC dc circuit charging format! This **could** blow the capacitor (if voltage rating exceeded) or an internal DBU transistor **could** blow on instantaneous over voltage! **NOT GOOD!!** But none of this happens if point **B** is used/available (again sometimes not available or wiring error).

Now, let us examine the same scenario with a DBU in place equipped with the Unique Multipurpose Circuit.

- If point **A** were brought out (all that was available *or wired wrong*) connected to **J1**, and power was applied, then, it should be clear the charging path for C1 is through the external (or even internal if low Hp DBU) load resistor, then up through D2, then into the upper plate of C1, out of the lower plate of C1 back to the Bridge 2 minus to form the series circuit current flow path. ***This is of course non problematic,*** utilizing the external (or internal) load absorbing resistor as a precharge resistor (dual purpose here). If point **B** were to be brought out, connected to **J1**, then of course, *it should be clear, again, the power up should be safe and uneventful.*
- The advantage of an externally connected DBU equipped with the Unique Circuit should be clear. It matters not if point **A** or **B** is used. And in the case where only point **A** exists, the advantage is even greater. *This type DBU is universal having obvious advantage.*

Variation 2: In this variation**, Bridge 1** would be present, but not **Bridge 2,** or it would have no AC input present. Note: For auxiliary purposes such as for AC cooling fans, there can exist other AC inputs not shown. In this variation, known as a Common DC Bus Supply arrangement (many good reasons to do this), **Bridge 1** would be *very high power rated.* Instead of (1) VFD, there would be many, each with its own motor with specific function, functioning overall as one big system. There are many examples in the world today utilizing this arrangement for good cause, which is beyond the necessary scope of discussion here.

- During initial system power up, there would typically be no VFDs connected for safety purposes. But the DBU (for very good purposes and cause) must be connected to this "master/solitary bridge node" point.
- It should be clear that C1 will have the same ***safe*** power up charging path as previously discussed, now being charged through **Bridge 1.**
- After initial power up, each of the VFDs will be individually connected in turn and the process repeated, until all are connected, again for safety purposes.
- **VERY IMPORTANTLY,** each VFD will use connection **point A** to **J1,** so as to make use of its own respective internal precharging resistor and contactor to safely charge up its large internal capacitor bank. <u>*This is an example of why* **point A** *is made available in a VFD!*</u> In this way, in this variation, each VFD could be added to or removed from a LIVE DC BUS……. which DOES HAPPEN. So, it should now be clear why point **A** is made available.

- It should also be clear the DBU in this case equipped with the Unique Circuit which requires no contactor/precharging resistor circuity offers clear advantage!
- A standard DBU with capacitors directly across the plus/minus would create the same BAD experience as spelled out above at applied power. Again, *the solution would have to be an ADD ON charging module, with the associated cost, space and other disadvantages previously mentioned.*
- A DBU equipped with the Unique Circuit **clearly** would be a preferred choice for reasons stated.

Now, let us cover the theory of operation of the Unique Circuit, while "transient protecting" transistor T1, utilizing automatic long wire stray inductance compensation.

- Assume the DBU (and load resistor) is powered up, sized accordingly and sufficiently to absorb the existing amount of regenerated energy (whilst present). At time 0, before DBU T1 turns on, C1 would be charged, its voltage equal to main VFD capacitance voltage.
- Assume long wires in use between VFD and special DBU. Assume and realize stray inductance (L stray) exists in the wires and is a significant amount, storing energy in this inductance amidst current flow. Note: *This* operating situation can normally only be tolerated by the *special DBU,* because the energy stored in the wire inductance will flow into the traditional DBU between "on" pulses, causing voltage resonations and ringing that can over voltage its capacitors and or cause transistor re-firing when it aught not do so. This scenario quite potentially causes bad catastrophic failures in the traditional DBU unless ADD ON capacitance (with/via charging module) is added to absorb the stored wire energy, alter(lower) the ringing resonating frequency etc. *It is quite possible the remedy may only be resorted to, or implemented.... after a costly failure.*
- Prior to first turn on of T1, C1 is at full charge (as noted) and thus has stored energy. L stray has zero current flowing and thus no stored energy. Recalling basic theory, C1 "Thevenizes" as a voltage source (low to zero impedance) and L stray as a current source (high impedance). When T1 **instantaneously** turns on, connecting Load Resistance across the DC Supply, L stray will initially appear "not there" (open circuit). However, C1 is a low impedance voltage source, thus a discharge current flow path instantaneously forms leaving C1 through D1(now on) down through Load Resistor and T1 into DC minus, into C1 minus *as a series circuit discharge path for C1*. So initially, all load resistor current is supplied by C1. Initially, the voltage on each side of L stray is equal, so no current can flow. However, as the voltage falls on C1, this causes voltage building across L stray

(and thus current building through it), since C1 is falling below the voltage level of the CAP in the VFD. * **Note: The value of C1 is magnitudes less than the value of VFD CAP.**

- So, what do we have at this moment? We have initial ohms law current from C equal to I (load r) = C1v/R ohms. So C1 is being drained and its voltage is falling. However, as stated, because of the decreasing C1 voltage, the voltage across L stray is increasing (thus its current is increasing). *So now, the sum current in R load is from C1* ***and*** *L stray.* C1 current starts high and falls, L stray current starts at zero and begins to rise (at a rate dependent upon how far C1v is falling). This process continues until the total current flowing in R is composed *ONLY* of L stray current, at which time, C1 current has reached zero and D1 ceases to conduct. ***Important note…. for a given value of R, how far C1v falls is very dependent on the value of L stray.** For example, if the exact DBU is transplanted into a system with less L stray, C1v will fall *less* in magnitude by the time its discharge current is zero. By the same token, if the same DBU is transplanted into a system with greater L stray, *C1 will* ***automatically*** *fall proportionately further* in voltage by the time its discharge current is zero. For a larger value of L stray, it takes a greater "voltage time product" expressed across it (vs a smaller value of L stray) for it to become the only current carrier into R load. The only thing that will cause more voltage to be expressed across L stray (needed) will be greater loss in C1v during this time. This can also be discussed in terms of energy surrendered by C1 versus the energy required to build in L stray, but that discussion is not necessary to gain understanding that C1v will fall more in a system with greater value of L stray.
- The shear fact that C1v falls more (and how much) in the presence of greater L stray is very important for what comes next, and reveals the beauty and **novel nature** of this circuit in terms of self-compensating for values of L stray.
- T1 on current = R load current = L stray current. C1 current =0. Equilibrium exists. ***C1v has fallen substantially below VFD CAP voltage*** and just sits there at a "holding voltage". *Nothing is draining C1 voltage at all.* **L stray current is maximum and thus its stored energy is maximum.**
- *It is also worth noting, that there is stray inductance within the load resistor, and its connected wires, especially if its wires are long (which can and will be the case if many thousands of watts are being dissipated).
- T1 now turns off. The current in L stray (DC lines) will not stop, and **WILL** continue to flow same direction **somewhere** until it no longer has current (or stored energy). The same is true for the inductance in the resistor and its wires. Where will it flow? Where will it surrender its stored energy? Since T1 turning off is *not* a

lossless event, some energy will be lost in T1 transitioning from on to off....but not a lot overall. The voltage will rise across T1 ***very*** quickly unabated! **Until**....until it reaches the *C1 "holding voltage" level...... plus the forward voltage diode drop of D2,* at which time this "pushing" inductive current flow will divert through D2(on) into C1. Since voltage cannot change instantly across a capacitor, its rate of rise will be determined by its value and the inductive "push" current. So suddenly, well below the VFD CAP voltage (at C1 holding voltage), the turn off voltage across T1 is limited and clamped to this *very safe voltage **BELOW*** the main DC supply!! **How novel and cool is that!!** The voltage rise across T1 abruptly changes and takes on this new greatly reduced "rate of rise" rate beginning far below the supply voltage**. **<u>Very protective for T1</u>** (the objective) *in the midst of a relatively high inductive setting.*

- So now the current flow path has been diverted from T1(off) into C1 through lower diode D2. Overall, it is from VFD + through L stray (DC supply wires), through the Load Resistor (and its associated inductance), through D2, into C1, leaving C1 minus back to VFD minus as the series circuit current flow path. Since the flow is through the Load Resistor, power and thus ***the stored wire energy*** is being **lost** in the process of charging C1!!. Based on component values, C1 can continue to charge and go above the voltage of VFD CAP by the time current into it (through L stray) is zero, but not very far, because of the "lossy charging path." When C1 charging stops, if C1 has charged above VFD voltage, then current now reverses. It comes out of C1, through upper diode D1, through L stray into VFD+. Now the path is mainly inductive and capacitive, *but energy is being lost in D1(on), ohmic value of wires etc.* This would typically discharge C1 slightly below VFD value (but not much) as its discharge current reaches zero. Current would then reverse again in the effort to charge C1 = to VFD, but this now (through R) again is energy lossy. This back-and-forth current flow process ***rapidly extinguishes*** and terminates due to the R losses, and C1v settles to = VFD voltage.
- To further emphasis a *related* automatic inductance compensation point, as noted, the higher the DC supply wire stray inductance, the further C1 will fall to its "*holding point"*. But this is totally ideal! The further it falls, it is now ***uniquely***, (in direct proportionate manner) perfectly, and best prepared as an "energy recipient" ....to take on ***more*** inductive energy and protect T1!! If the capacitor did not automatically fall further(remained = to VFDv) ..... the ensuing larger energy lump coming its way, could over pump C1v to the point of failure of T1. C1

would have to be much larger (in capacitance) to protect T1 otherwise. The benefits of not having to do so should be obvious and apparent.

- The converse is also true. If L stray is small, then C1v will not fall far, *but it need not fall far,* because the amount of forthcoming recipient energy is much lower. It should be clear the circuit automatically "presets" C1 "holding voltage" (as a function of L1 stray) so as to be an adaptive, "self-compensating", automatically "self-adjusting", "T1 protective" energy receiver.
- So, we have a highly effective T1 transient voltage protection circuit, *that in very novel and unique way,* self and automatically compensates for long wire inherent inductance, ***which utilizes the load resistor itself*** (verses an additional resistor for this purpose), as a loss producing (damping) component to eliminate transient ringing. A circuit allowed to ring WILL radiate/transmit this frequency and can easily INTERFERE with proper functioning of nearby system circuitry causing nuisance problems or failures! Any load that consumes power will have dampening effect. *In many applications, switching noise (ringing) limits exist… and must be adhered to.* This circuit provides compliance.
- Depending on any other power delivering application (or this one) to a load, the value of C1 would adjust based on power rating. But in this example, it would always be <u>*magnitudes less*</u> than the VFD CAP value.
- In further demonstration of this circuit functional versatility, if an application happens to have very low L stray, but high values of load circuit inductance, (or any other parameters dictate) then diodes D1 and D2 will act as "freewheeling" diodes, where at T1 turn off, they will carry the load "pushing" current round and round through the load (current will be reducing or reach zero) till T1 turns on again. But C1 will still limit any voltage transients as needed.
- As should be clear, there are A LOT of ***unique*** capabilities offered by this circuit, A LOT of functions going on within it, offering many benefits and advantages.

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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
63/616,829	**01/02/2024 1:42:22 AM ET**	-

Title of Invention

Sensor Less Dual Purpose Transistor Current Limiter and Fault Protector

Application Information

APPLICATION TYPE	Utility - Provisional Application under 35 USC 111(b)	PATENT #	-
CONFIRMATION #	4534	FILED BY	Timothy Atchison
PATENT CENTER #	63801019	FILING DATE	-
CUSTOMER #	-	FIRST NAMED INVENTOR	Timothy Atchison
CORRESPONDENCE ADDRESS	Timothy Atchison 353 Sunset Island Trail Gallatin, TN37066	AUTHORIZED BY	-

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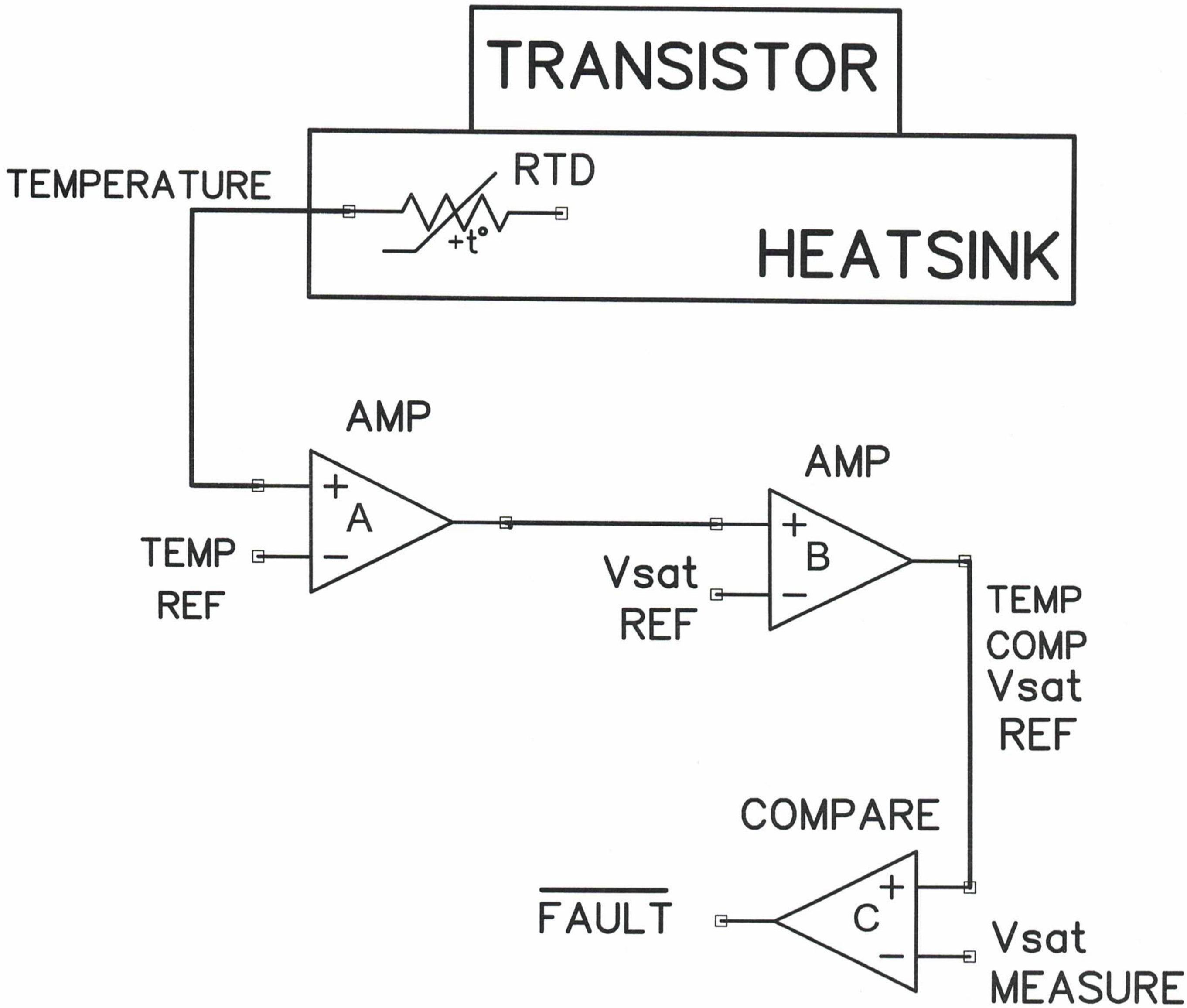
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Sensor Less Dual Purpose Transistor Current Limiter and Fault Protector

Preface: In today's world of high-Power Electronics such as found in AC or DC Motor Controllers etc., the IGBT transistor is the main workhorse when it comes to high current and high voltage switching applications (power MOSFETs are also used, but they have less voltage capacity). They are intended to switch currents into inductors (such as in Buck or Boost Regulators and the like), currents into motors (being inductive and resistive combined), or just into resistive loads such as resistors themselves, heating elements etc.

In some applications like current sources, or current controllers, there may be the need to limit the current during each transistor "on" state on a pulse-by-pulse basis. Other applications may need to limit the current *not* on a pulse-by-pulse basis, but on a "that is a bit too much current" (but not catastrophic) prechosen point. Each of these applications traditionally needs to make use of a current sensor device to monitor the current flowing and to thus "feedback" "limit points".

Transistors carry current in one direction only, so this makes them a DC current component. In AC currents, the sensing of it is very easy. Devices (sensors) such as current toroids are used. But these DO NOT work for DC currents. One then must traditionally resort to a "Hall Effect" device, which measures the magnetic field surrounding a current carrying wire (the field being proportional to current flow). But these devices are somewhat slow in reaction time, and thus not ideal when trying to limit a current rising extremely fast, *such as in the presence of a catastrophic load fault* (or commutation diode in a "continuous" current regulator application—not necessary here to explain commutation diode). One can also use a "sampling resistor" or shunt resistor, which is commonly used to drive older analogue meter movements. The voltage drop would typically be in the neighborhood of 50mv to represent max current in this "finely trimmed/calibrated very low ohmic value" resistor. But this sampling resistor can be in a "HOT" dangerous section of the overall circuit, making electronic monitoring of the tiny voltage drop across it very difficult, and add extra circuitry in an "electrically unisolated, non-groundable" part of the system.

Although the current limit process described above is very important and necessary in a given control scheme, there also needs to be some means present in a well-designed circuit to protect the transistor if a catastrophic extreme overload or short circuit is encountered. If a HALL EFFECT device is used, the current (in this fault case—very high di/dt) can reach enormous value during its sensing reaction time which could easily destroy/explode the IGBT.

Main: Consequently, I conceived a circuit that DOES NOT use current sensors of any type that addresses the above "sensor shortcomings", can be used in a cycle-by-cycle basis to limit currents, ***but in dual purpose manner***, will also protect the transistor if a catastrophic shorted/faulted load/fault current condition happens to occur…. which does occur.

For a moment, let us discuss the overload capability of the IGBT upon encountering an extreme situation. Compared to diodes and SCRs, the IGBT is somewhat delicate. Comparatively and technically speaking, they have a very low "I squared T" rating. *However, just like the diodes and SCRs, the transistor needs to have some form of protection in place.* In the case of protecting the diodes and SCRs, all a design engineer has to do is choose an "in line" fuse (proper type) whose "I squared T" rating is slightly less than that of either of these devices. When a short circuit situation comes along (which does---fault current) or other severe current overload, the fuse element is sacrificial and will melt first, thus protecting the device as desired. *Even the fastest semiconductor fuses today,* **when sized not to ever fatigue and blow** under "all" RMS load current conditions, (this would be nuisance fuse blowing) will not protect the IGBT when a short circuit fault current comes along. *The fuse can be coordinated such that in this case, there may* ***not*** *be a loud destructive explosion,* but it will not save and protect the IGBT under a worst-case fault condition.

There are electronic protection strategies that work or may work, but they have an inherent flaw. As such, and as very needed in the world today, I conceived this circuit that will "better protect with less stress" the IGBT in a bolted fault, dead short load condition, where depending on a high-speed fuse alone would not work. The typical protective strategy employed today to save the transistor in a dire encounter is referred to as a DESAT monitor approach. The current is not measured in this approach. The *voltage* across the transistor when it is on (via

gate command to be on) and carrying current is monitored. The detection circuit works by manner of when the voltage (only when on) *exceeds a set level (setpoint)*, there is an "assumption" made the device has experienced significant over current, triggering a protective fault.... device turn off command.

This "on" voltage is dependent on two things...the current it is carrying, *and the device temperature.* The problem is that the IGBT has a positive temperature coefficient associated with its "on" voltage (which is good for certain purposes). The hotter the device gets for a given fixed current, the greater the voltage drop across it.

To illustrate, for example, for a given device let us say it is rated for 500 amps. Let us say the device is in a piece of equipment rated 0 to 40 degrees C ambient (normal/typical). Let us say it is operating within its allowed current, at full load of the equipment, and the ambient temperature is at the upper end of published/rated equipment operating range (40 degrees C). The temperature of the transistor junction cannot (normally) go above 150 degrees C, so let us say it is at 135 degrees C. The voltage drop across the transistor will represent a worst-case scenario, and it will be at its greatest of all. Let us say the voltage drop across the transistor at this time is 2.5 V. Our "set" level will have to be greater than this to avoid nuisance shut down and to account for transistor "production lot" variation. Let us pick 3 V. This will coincide with a current (typically peak which will be high relative to steady state rating). Now let us operate the same equipment at the other end of its operating range (0 degrees C).

Now in protective mode, the setpoint of 3 V will equate to **far greater** cutoff current than previous, *up to 50% more or greater!* Not only will this greatly stress the device, but the *unnecessarily high* "let through" *cut off current* will have to be absorbed (in transient nature) by the bus structure surrounding the transistor, which could produce a transient overvoltage of the transistor in an insufficiently designed bus structure. These stresses and potential failure risks *can be avoided*, with the circuit I conceived that will limit each current on a pulse-by-pulse basis (during conduction) ... but will also prevent/minimize the *temperature phenomena* created "excessive" fault current at fault interrupt, experienced in the traditional approach.

What I conceived is a temperature feedback approach which automatically adjusts the *shutoff* ***setpoint*** up or down relative to the heatsink temperature (which the device temp follows). I use an RTD to track the device temperature and thus "temperature compensate" the setpoint…. a rise in temperature produces ***appropriate*** rise in setpoint and vice versa. The shut off circuit (monitoring the transistor on voltage) can be calibrated to shut off at a desired current (non-fault), and when the temperature changes, it will cut off at the same current (or very close), because the temperature change has been factored in. When it comes to ***fault current time***, this approach *greatly* reduces the "let through" current value (with less device stress and other potential risks) compared to the traditional method and will protect the device in a high di/dt short circuit fault current experience. Each device is different, so the setup is per device characteristics.

Features/Benefits

- Functions as a very fast acting "sensor less" current sensor
- Good for switching inductor, motor, or resistor/heating element loads
- Overcomes drawbacks of slower sensors or use of "shunt" resistor
- DC Current sensor not needed
- Greatly reduces "fault let through" currents minimizing risks, transients and device stress
- Minimal circuitry necessary to achieve
- Can be used also with MOSFETs as they have the same positive temperature coefficient of "on voltage"